AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method, comprising:

retrieving an instruction from a memory unit via an n-bit input path;

[partially] pre-decoding the instruction at a direct memory access unit;

providing the pre-decoded instruction from the direct memory access unit to a processing element via a q-bit output path, where $n < q$;

[completely] decoding the pre-decoded instruction at the processing element; and

executing the completely decoded instruction at the processing element.

2. (Original) The method of claim 1, wherein said providing comprises storing the pre-decoded instruction in memory local to the processing element.

3-4. (Canceled)

5. (Original) The method of claim 1, further comprising:

loading instructions into the memory unit during a boot-up process.

6. (Original) The method of claim 1, wherein the processing element is a reduced instruction set computer device.

7. (Original) The method of claim 6, wherein the pre-decoded instruction comprises execution control signals.

8. (Currently Amended) An apparatus, comprising:

an n-bit input path to receive an instruction from a memory unit;

a direct memory access unit including an instruction pre-decoder to [partially] pre-decode the received instruction;

[an] a q-bit output path to provide a [partially] pre-decoded instruction from the direct memory access unit, where $n < q$; and

a processor to receive the [partially] pre-decoded instruction from the q-bit output path and [completely] decode the [partially] pre-decoded instruction.

9. (Original) The apparatus of claim 8, further comprising:

the memory unit coupled to the input path.

10. (Canceled)

11. (Previously Presented) The apparatus of claim 8, wherein the processing element includes a local memory to store the pre-decoded instruction.

12. (Previously Presented) The apparatus of claim 8, including a plurality of processing elements, each processing element being associated with a direct memory access unit that includes an instruction pre-decoder.

13. (Canceled)

14. (Previously Presented) The apparatus of claim 8, wherein the direct memory access unit, the memory unit, and the processing element are formed on an integrated circuit.

15. (Previously Presented) The apparatus of claim 8, wherein the processing element is a reduced instruction set computer device having an instruction pipeline.

16. (Currently Amended) An article, comprising:

a computer-readable storage medium having stored thereon instructions that when executed by a machine result in the following:

retrieving an instruction from a memory unit via an n-bit input path,

[partially] pre-decoding the instruction at a direct memory access unit, and

providing via a q-bit output path the pre-decoded instruction from the direct memory access unit to a processing element to be [completely] decoded, where $n < q$.

17. (Original) The article of claim 16, wherein said providing comprises storing the pre-decoded instruction in memory local to the processing element.

18-20. (Canceled)

21. (Currently Amended) A system, comprising:

a multi-directional antenna;

an apparatus having a direct memory access unit that includes:

an n-bit input path to receive an instruction from a memory unit,

an instruction pre-decoder to [partially] pre-decode the instruction, and

[an] q-bit output path to provide a pre-decoded instruction, where $n < q$; and

a processor to receive and [completely] decode the [partially] pre-decoded instruction received via the q-bit output path.

22. (Original) The system of claim 21, wherein the apparatus is a digital base band processor.

23. (Original) The system of claim 22, wherein the digital base band processor is formed as a system on a chip.

24. (Original) The system of claim 21, wherein the system is a code-division multiple access base station.